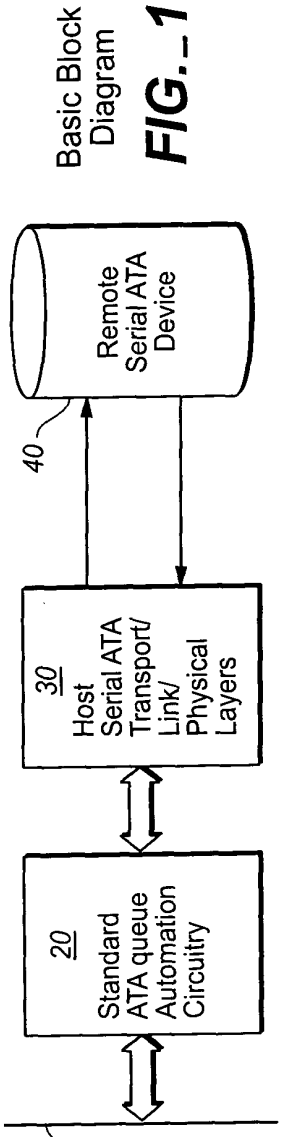
Basic Block Diagram

FIG._1



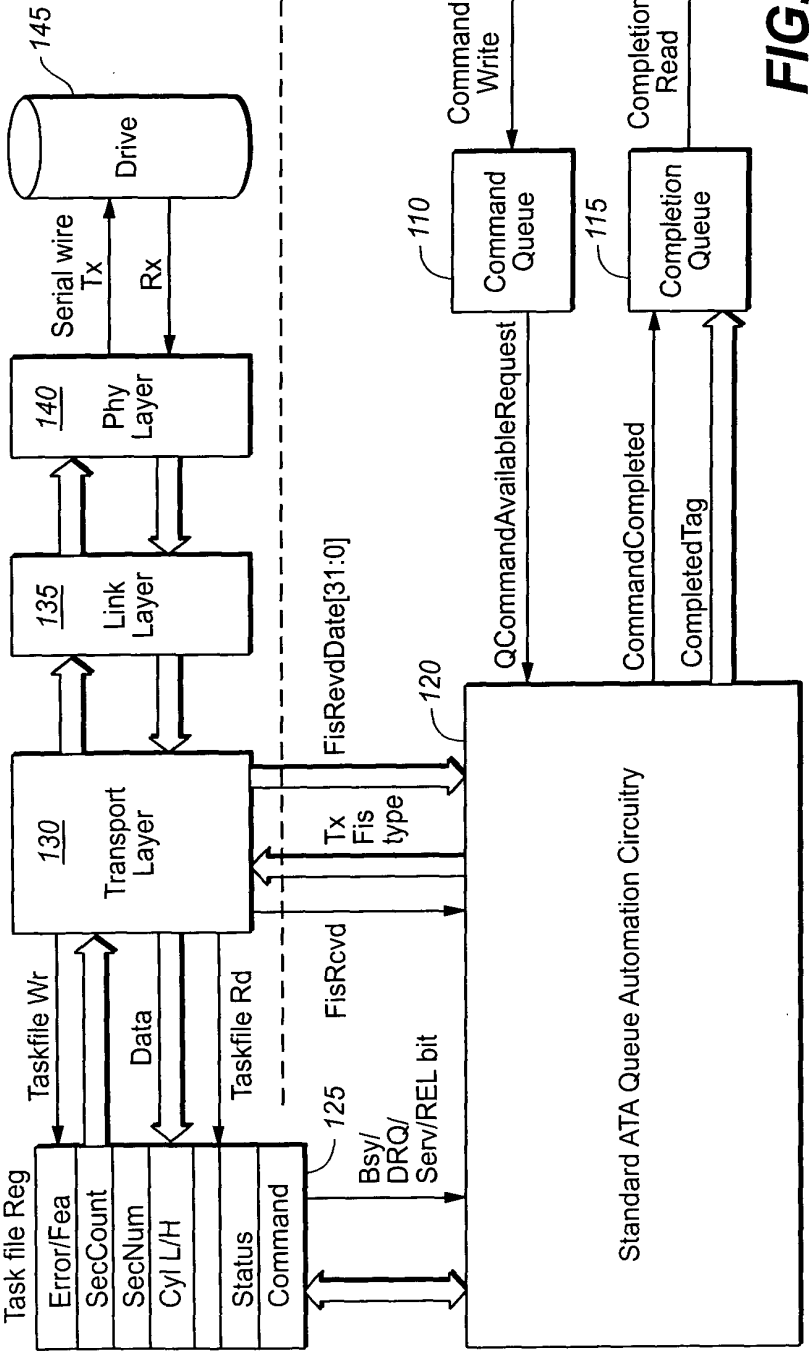


FIG._2

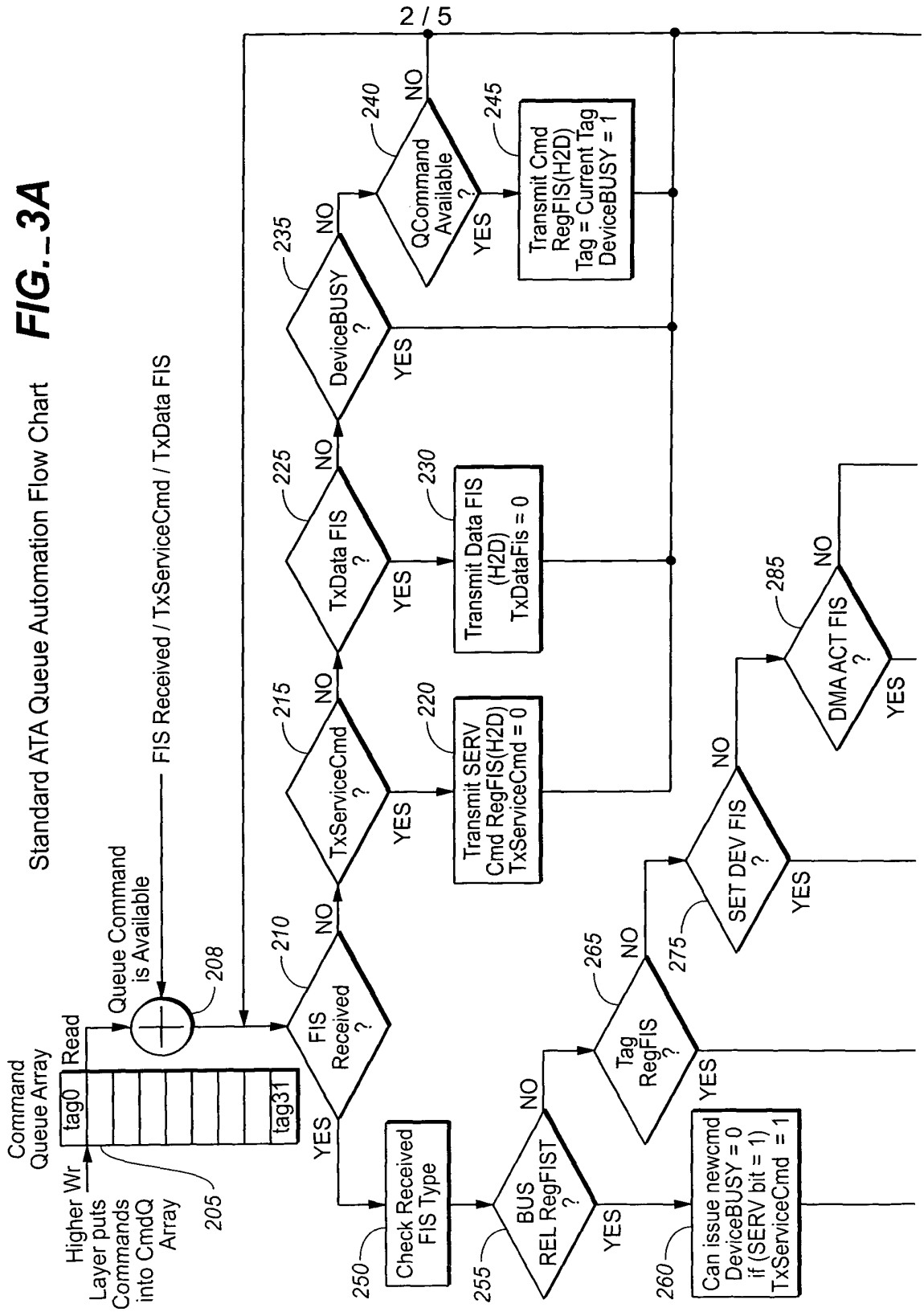

Standard ATA Queue Automation Flow Chart
2 / 5
Command Queue Array
Read
tag0
tag31
Higher Wr
Layer puts Commands into CmdQ Array
205
Queue Command is Available
FIS Received / TxServiceCmd / TxData FIS
208
FIS Received ?
210
YES
NO
Check Received FIS Type
250
TxServiceCmd ?
215
Transmit SERV Cmd RegFIS(H2D) TxServiceCmd = 0
220
TxData FIS ?
225
Transmit Data FIS (H2D) TxDataFis = 0
230
DeviceBUSY ?
235
QCommand Available ?
240
Transmit Cmd RegFIS(H2D) Tag = Current Tag DeviceBUSY = 1
245
BUS REL RegFIST ?
255
Can issue newcmd DeviceBUSY = 0 if (SERV bit = 1) TxServiceCmd = 1
260
Tag RegFIS ?
265
SET DEV FIS ?
275
DMA ACT FIS ?
285

FIG._3A

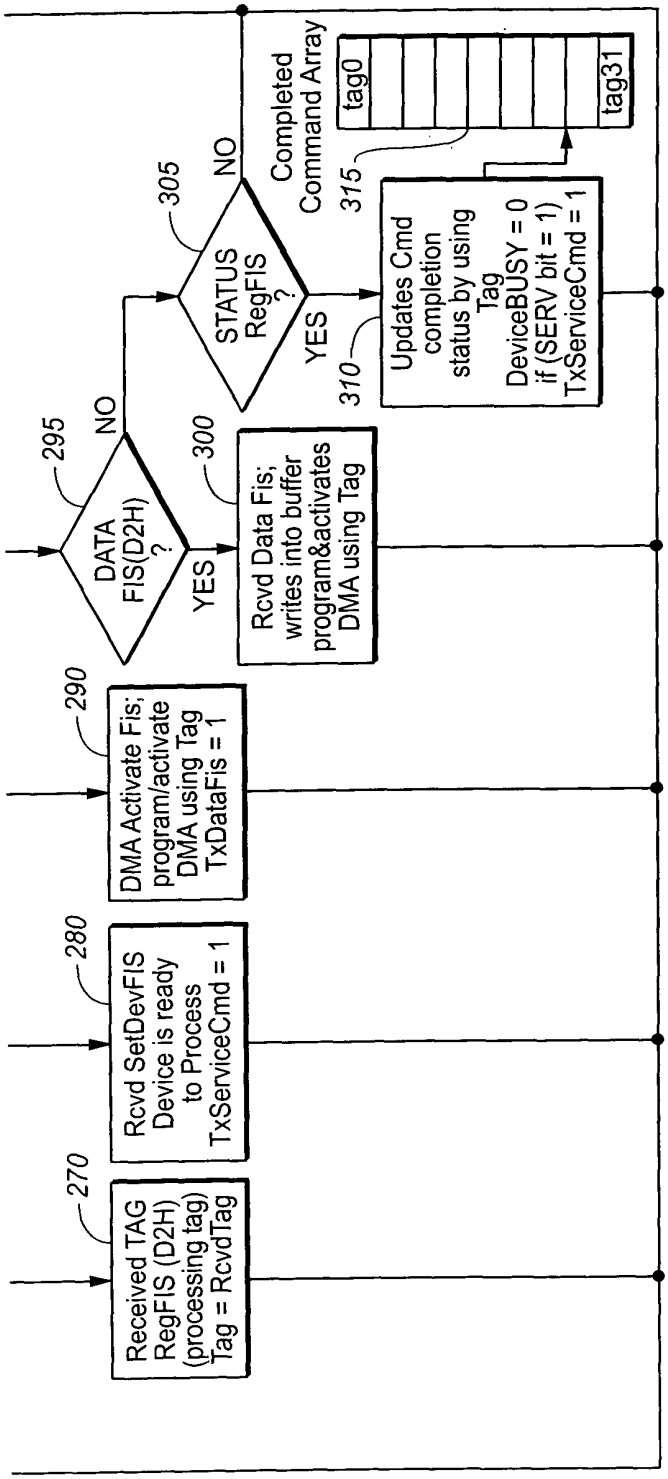


FIG._3B

FIG._3

FIG._3A

FIG._3B

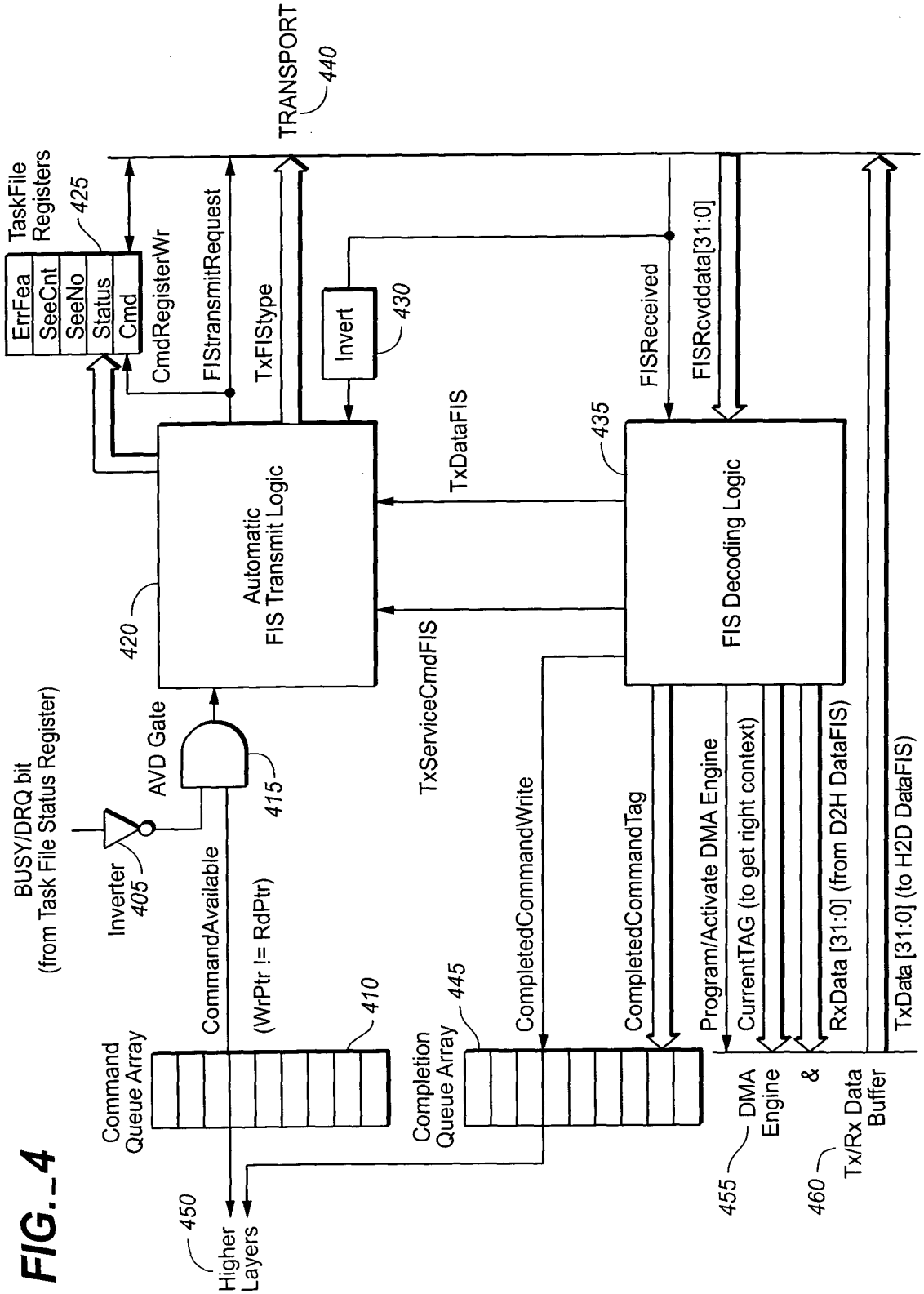

TRANSPORT
440
TaskFile Registers
425
ErrFea
SeeCnt
SeeNo
Status
Cmd
CmdRegisterWr
FIStransmitRequest
TxFIStype
Invert
430
TxDataFIS
FISReceived
FISRcvddata[31:0]
435
Automatic FIS Transmit Logic
420
FIS Decoding Logic
TxServiceCmdFIS
BUSY/DRQ bit (from Task File Status Register)
AVD Gate
415
Inverter
405
CommandAvailable
(WrPtr != RdPtr)
410
CompletedCommandWrite
CompletedCommandTag
Program/Activate DMA Engine
CurrentTAG (to get right context)
RxData [31:0] (from D2H DataFIS)
TxData [31:0] (to H2D DataFIS)
Command Queue Array
Completion Queue Array
445
450
Higher Layers
455
DMA Engine
&
460
Tx/Rx Data Buffer

FIG._4

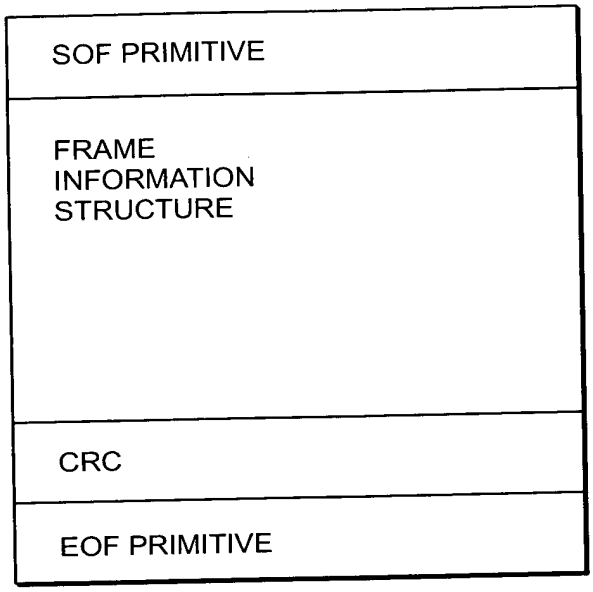

SOF PRIMITIVE
FRAME
INFORMATION
STRUCTURE
CRC
EOF PRIMITIVE

FIG._5